

What is claimed:

1           1.       A method for manufacturing a semiconductor device, the method comprising  
2 the steps of:

3           (a) forming a gate dielectric layer;

4           (b) forming a first conduction layer on the gate dielectric layer;

5           (c) forming a first upper layer comprising a material different from the first  
6 conduction layer on the first conduction layer;

7           (d) forming a second upper layer comprising a material different from the first upper  
8 layer on the first upper layer

9           (e) forming sidewall spacers on side walls of the first conduction layer, the first  
10 upper layer and the second upper layer;

11           (f) forming an insulation layer that covers the second upper layer and the sidewall  
12 spacers;

13           (g) planarizing the insulation layer until an upper surface of the second upper layer is  
14 exposed;

15           (h) removing the second upper layer;

16           (i) removing the first upper layer to form a recessed section between the sidewall  
17 spacers; and

18           (j) forming a second conduction layer in the recessed section to form a gate electrode  
19 that includes at least the first conduction layer and the second conduction layer.

1           2.       A method for manufacturing a semiconductor device according to claim 1,  
2 wherein the step (h) is conducted by an etching method, and in the step (h), a ratio of an  
3 etching rate of the second upper layer with respect to an etching rate of the first upper layer  
4 is two or greater.

1           3.       A method for manufacturing a semiconductor device according to claim 1,  
2 wherein the step (i) is conducted by an etching method, and in the step (i), a ratio of an  
3 etching rate of the first upper layer with respect to an etching rate of the first conduction  
4 layer is two or greater.

1           4.       A method for manufacturing a semiconductor device according to claim 1,  
2 wherein the first upper layer is formed from silicon nitride and the second upper layer is  
3 formed from polysilicon.

1           5.       A method for manufacturing a semiconductor device according to claim 1,  
2 further comprising, after step (i), forming a barrier layer between the first conduction layer  
3 and the second conduction layer.

1           6.       A method for manufacturing a semiconductor device according to claim 1,  
2 further comprising, after step (i), forming a barrier layer between the first conduction layer  
3 and the second conduction layer, and forming the barrier layer between the second  
4 conduction layer and the sidewall spacers.

1           7.       A method for manufacturing a semiconductor device, the method comprising  
2 the steps of:

3           (a) forming a gate dielectric layer;

4           (b) forming a first conduction layer on the gate dielectric layer;

5           (c) forming an upper layer on the first conduction layer, at least a lower portion of  
6 the upper layer comprising a material different from at least an upper portion of the first  
7 conduction layer;

8           (d) forming sidewall spacers on side walls of the first conduction layer and the upper  
9 layer;

10          (e) forming an insulation layer that covers the upper layer and the sidewall spacers;

- 11 (f) planarizing the insulation layer until an upper surface of the upper layer is  
12 exposed;
- 13 (g) removing the upper layer to form a recessed section between the sidewall spacers  
14 on an upper portion of the first conduction layer; and
- 15 (h) forming a second conduction layer in the recessed section to form a gate  
16 electrode that includes at least the first conduction layer and the second conduction layer.

1 8. A method for manufacturing a semiconductor device according to claim 7,  
2 wherein the step (g) is conducted by an etching method, and in the step (g), a ratio of an  
3 etching rate of at least the lower portion of the upper layer with respect to an etching rate of  
4 the at least upper portion of the first conduction layer is two or greater.

1 9. A method for manufacturing a semiconductor device according to claim 7,  
2 wherein the first conduction layer is formed from a polysilicon layer.

1 10. A method for manufacturing a semiconductor device according to claim 7,  
2 wherein the second conduction layer comprises a material selected from the group  
3 consisting of a metal, a metal alloy and a metal compound.

1 11. A method for manufacturing a semiconductor device according to claim 7,  
2 further comprising, after step (g), forming a barrier layer between the first conduction layer  
3 and the second conduction layer.

1 12. A method for manufacturing a semiconductor device according to claim 7,  
2 further comprising, after step (g), forming a barrier layer between the first conduction layer  
3 and the second conduction layer, and forming the barrier layer between the second  
4 conduction layer and the sidewall spacers.

13. A method for manufacturing a semiconductor device, the method comprising:  
forming a gate dielectric layer;  
forming a first conduction layer on the gate dielectric layer;  
forming an upper layer on the first conduction layer, the upper layer comprising a material different from that of the first conduction layer;  
forming sidewall spacers on side walls of the first conduction layer and the upper layer;  
removing the upper layer to form a recessed section between the sidewall spacers and above at least part of the first conduction layer; and  
forming a second conduction layer in the recessed section to form a gate electrode comprising the at least part of the first conduction layer and the second conduction layer.

1 14. A method for manufacturing a semiconductor device according to claim 13,  
2 further comprising, after step (g), forming a barrier layer between the first conduction layer  
3 and the second conduction layer.

1 15. A method for manufacturing a semiconductor device according to claim 13,  
2 further comprising, after step (g), forming a barrier layer between the first conduction layer  
3 and the second conduction layer, and forming the barrier layer between the second  
4 conduction layer and the sidewall spacers.

1 16. A method for manufacturing a semiconductor device according to claim 13,  
2 wherein the first conduction layer and second conduction layer comprises materials having  
3 different compositions.

1 17. A method for manufacturing a semiconductor device according to claim 13,  
2 wherein the first conduction layer comprises polysilicon and the second conduction layer  
3 comprises a material selected from the group consisting of a metal, a metal alloy and a metal  
4 compound.

1 18. A semiconductor device comprising:  
2 a field effect transistor, the field effect transistor including a gate dielectric layer, a  
3 gate electrode, sidewall spacer regions, a source region, and a drain region, wherein  
4 the gate electrode includes a first conduction layer and a second conduction layer,  
5 the first conduction layer is formed on the gate dielectric layer,  
6 the second conduction layer is formed above the first conduction layer,  
7 the sidewall spacer regions are formed on side walls of the gate electrode,  
8 an insulation layer is provided adjacent to the sidewall spacer regions, and  
9 a barrier layer is provided between the first conduction layer and the second  
10 conduction layer and between the second conduction layer and the sidewall spacer.

1 19. A semiconductor device comprising:  
2 a field effect transistor, the field effect transistor including a gate dielectric layer, a  
3 gate electrode, sidewall spacers, a source region, and a drain region, wherein  
4 the gate electrode includes a first conduction layer and a second conduction layer,  
5 the first conduction layer is formed on the gate dielectric layer,  
6 the second conduction layer is formed above the first conduction layer,  
7 the sidewall spacers are formed adjacent to side walls of the gate electrode, and  
8 an insulation layer is provided adjacent to the sidewall spacers, wherein an upper  
9 surface of the insulation layer and an upper surface of the second conduction layer are  
10 substantially at the same level.

1 20. A method for manufacturing a semiconductor device according to claim 18,  
2 wherein the first conduction layer is formed from a polysilicon layer.

1 21. A method for manufacturing a semiconductor device according to claim 18,  
2 wherein the second conduction layer comprises at least one material selected from the group  
3 consisting of a metal, a metal alloy and a metal compound.